CLAIMS

Please amend the claims as follows:

1. (currently amended) A computer implemented method for utilizing a signal delay model for determining an interconnect delay at a node in an interconnect modeled as a resistive-capacitive (RC) tree having a plurality of nodes, said method comprising:

determining an equivalent effective capacitance value for a downstream load seen at said node, wherein said determining an equivalent effective capacitance includes:

utilizing a pi-model to model said downstream load; and

determining an Elmore delay value for said node;

wherein said equivalent effective capacitance (Ceff) is characterized by:

$$Ceff = Cfj(1 - e^{-T/\tau dj})$$

wherein Cfj is a far-end capacitance of said pi-model at said node, T is the Elmore delay at said node and τdj is a resistance of said pi-model (Rdj) multiplied by Cfj; and

utilizing said equivalent effective capacitance value to calculate said interconnect delay at said node.

2. (original) The method as recited in Claim 1, further comprising performing a bottom-up tree traversal to compute the first three admittance moments for each of said plurality of nodes in said interconnect.

3. (original) The method as recited in Claim 1, wherein said determining an equivalent effective capacitance value includes determining interconnect delays for nodes in said interconnect preceding said node.

4-6. (canceled)

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7. (currently amended) The method as recited in Claim 1 [[6]], wherein said utilizing said equivalent effective capacitance value includes calculating said interconnect delay at said node utilizing an effective capacitance metric (ECM) delay model, wherein said ECM delay model is characterized by:

$$ECMj = ECMp(j) + Rj(Cj + Cnj + Cfj(1 - e^{-T/\tau dj}))$$

wherein ECMp(j) is [[the]] a computed ECM delay at [[the]] a preceding node immediately preceding said node, Rj is [[the]] a resistance between said node and said preceding node, Cj is [[the]] a capacitance to ground at said node and Cnj is [[the]] a near-end capacitance of said pi-model at said node.

8. (currently amended) A data processing system, comprising:

a processor;

means for determining an equivalent effective capacitance value for a downstream load seen at a node in an interconnect modeled as a resistive-capacitive (RC) tree having a plurality of nodes, wherein said determining an equivalent effective capacitance includes:

utilizing a pi-model to model said downstream load; and

determining an Elmore delay value for said node;

wherein said equivalent effective capacitance (Ceff) is characterized by:

$$Ceff = Cfj(1 - e^{-T/\tau dj})$$

wherein Cfj is a far-end capacitance of said pi-model at said node, T is the Elmore delay at said node and τdj is a resistance of said pi-model (Rdj) multiplied by Cfj; and

means for utilizing said equivalent effective capacitance value to calculate an interconnect delay at said node.

9. (original) The data processing system as recited in Claim 8, further comprising means for performing a bottom-up tree traversal to compute the first three admittance moments for each of said plurality of nodes in said interconnect.

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10. (original) The data processing system as recited in Claim 8, wherein said means for determining an equivalent effective capacitance value includes means for determining interconnect delays for nodes in said interconnect preceding said node.

11-13. (canceled)

14. (currently amended) The data processing system as recited in Claim 8 [[13]], wherein said means for utilizing said equivalent effective capacitance value includes means for calculating said interconnect delay at said node utilizing an effective capacitance metric (ECM) delay model, wherein said ECM delay model is characterized by:

$$ECMj = ECMp(j) + Rj(Cj + Cnj + Cfj(1 - e^{-T/\tau dj}))$$

wherein ECMp(j) is [[the]] a computed ECM delay at [[the]] a preceding node immediately preceding said node, Rj is [[the]] a resistance between said node and said preceding node, Cj is [[the]] a capacitance to ground at said node and Cnj is [[the]] a near-end capacitance of said pi-model at said node.

15. (currently amended) A computer program product, comprising:

a computer-readable medium having stored thereon computer executable instructions for implementing a method for determining an interconnect delay at a node in an interconnect modeled as a resistive-capacitive (RC) tree having a plurality of nodes, said computer executable instructions when executed perform the steps of:

determining an equivalent effective capacitance value for a downstream load seen at said node, wherein said determining an equivalent effective capacitance includes:

utilizing a pi-model to model said downstream load; and

determining an Elmore delay value for said node;

wherein said equivalent effective capacitance (Ceff) is characterized by:

$$Ceff = Cfj(1 - e^{-T/\tau dj})$$

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wherein Cfj is a far-end capacitance of said pi-model at said node, T is the Elmore delay at said node and τdj is a resistance of said pi-model (Rdj) multiplied by Cfj; and

utilizing said equivalent effective capacitance value to calculate said interconnect delay at said node.

16. (original) The computer program product as recited in Claim 15, further comprising performing a bottom-up tree traversal to compute the first three admittance moments for each of said plurality of nodes in said interconnect.

17. (original) The computer program product as recited in Claim 15, wherein said determining an equivalent effective capacitance value includes determining interconnect delays for nodes in said interconnect preceding said node.

18-20. (canceled)

21. (currently amended) The computer program product as recited in Claim 15 [[20]], wherein said utilizing said equivalent effective capacitance value includes calculating said interconnect delay at said node utilizing an effective capacitance metric (ECM) delay model, wherein said ECM delay model is characterized by:

$$ECMj = ECMp(j) + Rj(Cj + Cnj + Cfj(1 - e^{-T/\tau dj}))$$

wherein ECMp(j) is [[the]] a computed ECM delay at [[the]] a preceding node immediately preceding said node, Rj is [[the]] a resistance between said node and said preceding node, Cj is [[the]] a capacitance to ground at said node and Cnj is [[the]] a near-end capacitance of said pi-model at said node.

22. (currently amended) A program product comprising a computer-readable medium including program code for implementing a method for determining an interconnect delay at a node in an interconnect modeled as a resistive-capacitive (RC) tree having a plurality of nodes, wherein said program code causes a data processing system to perform the steps of:

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determining an equivalent effective capacitance value for a downstream load seen at said node, wherein said determining includes determining interconnect delays for nodes in said interconnect preceding said node;

utilizing said equivalent effective capacitance value to calculate said interconnect delay at said node, wherein said equivalent effective capacitance (Ceff) is characterized by:

$$Ceff = Cfj(1 - e^{-T/\tau dj})$$

wherein Cfj is [[the]] a far-end capacitance of [[said]] a pi-model at said node to model said downstream load, T is [[the]] an Elmore delay at said node and τdj is [[the]] a resistance of said pi-model (Rdj) multiplied by [[Cfi.]] Cfj.

23. (currently amended) The program product of Claim 22, wherein utilizing said equivalent effective capacitance value to calculate said interconnect delay includes calculating said interconnect delay at said node utilizing an effective capacitance metric (ECM) delay model, wherein said ECM delay model is characterized by:

$$ECMj = ECMp(j) + Rj(Cj + Cnj + Cfj(1 - e^{-T/\tau dj}))$$

wherein ECMp(j) is [[the]] a computed ECM delay at [[the]] a preceding node immediately preceding said node, Rj is [[the]] a resistance between said node and said preceding node, Cj is [[the]] a capacitance to ground at said node and Cnj is [[the]] a near-end capacitance of said pi-model at said node.

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